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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Satoshi TAKANO

Application No.: 09/819,696

Docket No.: 109107

Filed: March 29, 2001

For: SEMICONDUCTOR MANUFACTURING METHOD, SUBSTRATE PROCESSING
METHOD, AND SEMICONDUCTOR MANUFACTURING APPARATUS



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REQUEST FOR CORRECTION OF PALM RECORDS

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Respectfully submitted,

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Date: July 30, 2001

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APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
09/819,690	03/29/2001	2812	1000	109107	7	8	5

CONFIRMATION NO. 3148

UPDATED FILING RECEIPT



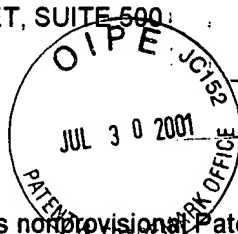
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Applicant(s)

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→ NAKANO-KU

Domestic Priority data as claimed by applicant

→ Assignment for Published Patent Application
HITACHI KOKUSAI ELECTRIC INC.

Foreign Applications

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N n-Publication Request: No

Early Publication Request: No

Title

Semiconductor manufacturing method, substrate processing method, and semiconductor manufacturing apparatus

Preliminary Class

438



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CONFIRMATION NO. 3148

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APPLICANTS Satoshi Takano, Nakand-Ku, JAPAN; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** JAPAN 2000-91642 03/29/2000 JAPAN 2001-60136 03/05/2001				
IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 05/05/2001				
Foreign Priority claimed <input checked="" type="checkbox"/> yes <input type="checkbox"/> no 35 USC 119 (a-d) conditions <input type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance Verified and Acknowledged <u> </u> Examiner's Signature Initials		STATE OR COUNTRY JAPAN	SHEETS DRAWING 7	TOTAL CLAIMS 8
INDEPENDENT CLAIMS 5				
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TITLE Semiconductor manufacturing method, substrate processing method, and semiconductor manufacturing apparatus				
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